In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method of image data processing comprising the steps of:

dividing an image into a plurality of two dimensional tiles, each tile ~~having~~ composed of a first predetermined number of ~~image~~ pixels adjacently disposed in ~~a single~~ each scan line ~~and~~ of a second predetermined number of adjacent scan lines;

storing image data in a memory having data words of a predetermined data width, each data word including said first predetermined number of ~~image~~ pixels adjacently disposed ~~on~~ in a single scan line, a set of said second predetermined number of consecutive data words corresponding to a two dimensional tile of ~~an~~ the image whereby adjacent data words include ~~image~~ pixels of adjacent scan lines;

transferring a tile of image data from the memory to a cache;

performing image operations upon said tile of image data transferred to the cache; and

transferring said tile of image data from the cache to the memory.

2. (Previously Amended) The method of claim 1, wherein:

said steps of transferring a tile of image data from the memory into the cache, performing image operations upon said tile of image data transferred to the cache, and transferring said tile of image data from the cache to the memory are repeated for each tile of image data.

3. (Previously Amended) The method of claim 1, wherein:

said steps of transferring a tile of image data from the memory into the cache, performing image operations upon said tile of image data transferred to the cache, and transferring said tile of image data from the cache to the memory are performed by different data processors for different tiles.

4 (Previously Amended) The method of claim 1, wherein:

said image operations includes read, modify and write of individual pixels within a data word.

5. (Currently Amended) An image data processing system comprising:

a memory storing image data having data words of a predetermined data width, each data word including a first predetermined number of ~~image~~ pixels adjacently disposed on a single scan line, a set of a second predetermined number of consecutive data words corresponding to a two dimensional tile of said first predetermined number of ~~image~~ pixels and said second predetermined number of scan lines of an image whereby adjacent data words include ~~image~~ pixels of adjacent scan lines;

a tile cache capable of storing a tile of image data from said memory;

a data processing apparatus connected to said memory and said tile cache, said data processing apparatus programmed to

transfer a tile of image data from said memory into said tile cache,

perform an image operation upon said tile of image data transferred to said tile cache, and

transfer that tile of image data from said tile cache to said memory.

6. (Previously Amended) The image data processing system of claim 5, wherein:

said data processing apparatus is further programmed to sequentially operate upon different tiles of image data.

7. (Previously Amended) The image data processing system of claim 5, further comprising:

a second data processing apparatus connected to said memory and said tile cache, said second data processing apparatus programmed to

transfer a tile of image data from said memory to said tile cache,

perform an image operation upon said tile of image data transferred to said tile cache, and

transfer that tile of image data from said tile cache to said memory; and

wherein said data processing apparatus and said second data processing apparatus are programmed to operate upon different tiles of image data simultaneously.

8. (Currently Amended) The method of claim 1, wherein:

said step of transferring a tile of image data from the memory to a cache includes making said second predetermined number of page mode ~~DRAM~~ dynamic random access memory (DRAM) accesses; and

said step of transferring said tile of image data from the cache to the memory includes making said second predetermined number of page mode DRAM accesses.

9. (Currently Amended) The image data processing system of claim 5, wherein:

said memory includes a DRAM supporting page mode accesses; and

said data processing apparatus is further programmed to

transfer a tile of image data from said memory into said tile cache via said second predetermined number of page mode ~~DRAM~~ dynamic random access memory (DRAM) accesses, and

transfer that tile of image data from said tile cache to said memory via said second predetermined number of page mode DRAM accesses.